16K Memory for VZ-300 Computer

This 16K expansion can be built for considerably less than commercial versions. It comprises two 8K x 8 6264 CMOS static RAMs, a 74HC138 1-of-8 decoder and a 4008 4-bit adder.

IC3 and IC4 provide decoding of the A11 to A14 memory addresses to select IC1 and IC2 via the CS1-bar chip select inputs. The Y0 and Y1 outputs of IC3 ensure that when IC1 is selected IC2 is deselected and conversely, when IC2 is selected IC1 is deselected. A15 is used to select both IC1 and IC2 via the CS2 chip selects.

The MREQuest-bar line is used to enable IC3 via the G2A-bar and G2B-

bar inputs.

Read and Write (RD-bar and WR-bar) lines select the Write Enable-bar (WE-bar) and Output Enable-bar (OE-

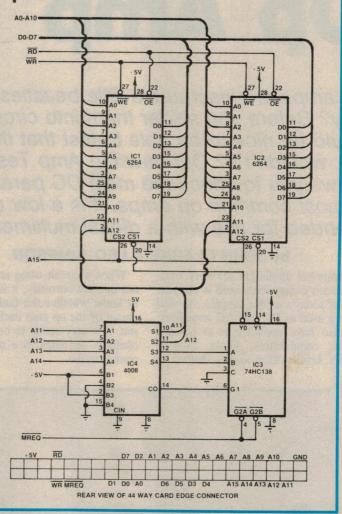
bar) of both IC1 and IC2.

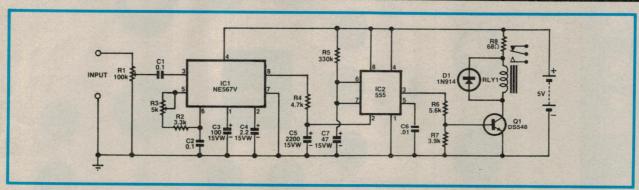
Data lines D0 to D7 connect to the D0 to D7 lines of both IC1 and IC2. For the memory, A0 to A10 connect directly to the A0 to A10 lines of IC1 and IC2, while A11 and A12 connect via IC4.

Construction can be wire wrap or on Veroboard. A 44-way 2.54mm (0.1 inch) edge connector connects the memory expansion to the VZ-300 computer. The connections for this bus are shown.

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on pin 2 of IC2, the 2kHz tone must be transmitted for at least five seconds to activate the relay. This long time constant provides protection against false triggering.

When setting up, adjust R1 first to eliminate breakthrough on strong sig-

nals, then adjust R3 for maximum sensitivity.

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Editor's note: a 2kHz encoder is required for use with the above circuit. A

555 timer IC wired in astable mode and driving a miniature loudspeaker should do the trick. Readers are also advised that a complete tone encoder/decoder project for amateurs and CBers will be published in the near future.